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10/511,566	04/13/2005	Jurgen Leib	2133.063USU	4191

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/511,566	LEIB ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32 and 34-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32 and 34-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

Claims 23, 26-27, 31, & 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada (US 2002/0019069).

Re claim 23, Wada discloses (Fig 1) an electronic module (1) comprising:

a substrate (6) having a first substrate side (A) and a second substrate side (B) opposite to the first substrate side ([0073] ln 6);

one or more semiconductor structures (13) being disposed on the first substrate side ([0073] ln 4-5);

a glass layer (9; [0077]) being deposited on the first substrate side; and

a plurality of etched pits (4) and line contacts (8) being defined on the second substrate side ([0074]).

The product-by-process limitation "vapor deposited" has not been given patentable weight. See MPEP § 2113.

Re claim 26, Wada discloses (Fig 1) the second substrate side is thinned (interpreted as made to the desired thinness).

The product-by-process limitation "after the glass layer is deposited on the first substrate side" has not been given patentable weight. See MPEP § 2113.

Re claim 27, Wada discloses (Fig 9) a passivation layer (26; [0136] ln 5) on the second substrate side.

Re claim 31, Wada discloses (fig 1) line contacts (8) that are connected to the one or more semiconductor structures ([0074] ln 6-8) on the first substrate side.

Re claim 32, Wada discloses (Fig 1) a ball grid array (24) at the line contacts.

Claim Rejections - 35 USC § 103

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada as applied to claim 23 above, and further in view of Camlibel (US 4,374,391).

Re claim 24, Wada differs from the claimed invention only in not disclosing a second glass layer on the second substrate side.

Camlibel discloses (Fig 5) an analogous device (60) with a glass layer (68) deposited on the back side.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel by depositing a glass layer on the second substrate side; at least to protect the surface (Camlibel: col 3 ln 46).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Camlibel and Xu (US 6,111,270).

Re claim 25, Wada discloses (Fig 1) an electronic module (1) comprising:

a substrate (6) having a first substrate side (A) and a second substrate side (B) opposite to the first substrate side ([0073] ln 6);

one or more semiconductor structures (13) being disposed on the first substrate side ([0073] ln 4-5);

a glass layer (9; [0077]) being deposited on the first substrate side; and

a plurality of etched pits (4) and line contacts (8) being defined on the second substrate side ([0074]).

The product-by-process limitation "vapor deposited" has not been given patentable weight. See MPEP § 2113.

Wada differs from the claimed invention only in not disclosing a plastic layer on a surface of the glass layer opposite the substrate.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 ln 51-53).

Xu discloses a dielectric stack of layers forming a partial mirror to reflect light (col 3 ln 35-44).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu to comprise a plastic layer on a surface of the glass layer opposite the substrate; at least to reduce surface reflection.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada as applied to claim 23 above, and further in view of Butt (US 4,889,960).

Re claim 28, Wada differs from the claimed invention in not disclosing the glass layer comprises a mixed layer of inorganic and organic constituents.

Butt discloses (Fig 1) electronic modules encapsulated with organic-reinforced glass (col 2 ln 67 – col 3 ln 6) to reinforce the glass (col 5 ln 11-15).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Butt by including organic constituents in the inorganic constituents of the glass; at least to reinforce the glass.

Claims 29 & 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada as applied to claim 23 above, and further in view of Camlibel and Xu.

Re claim 29, Wada differs from the claimed invention in not disclosing a plurality of glass layers.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 ln 51-53).

Xu discloses a dielectric stack of layers forming a partial mirror to reflect light (col 3 ln 35-44).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu by forming the glass layer from a plurality of glass layers; at least to reduce surface reflection.

Re claim 30, Wada as modified above discloses individual layers of the plurality of glass layers have different compositions (Xu: col 3 ln 37-39).

Claims 1-7, 9-14, 16-21 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Camlibel.

Re claim 1, Wada discloses (Figs 6-9) a process for forming a housing for electronic modules, comprising the steps of:

providing a substrate (5; [0083] ln 1-2) having one or more regions, the one or more regions having a structure of semiconductor structure (13; [0083] ln 4), the substrate having at least a first substrate side (B; [0084] ln 1-3) to be encapsulated and an underside (A);

coating the first substrate side with a glass layer (Fig 9: 9; [0113] ln 1-2);

thinning the substrate (interpreted as making to the desired thinness, which is inherent) on the underside;

producing etching pits (Fig 6E-7G: 4; [0093] ln 1-2) on the underside;

producing line contacts (Fig 8A: 8; [0098] ln 4-5) on the underside.

Wada differs from the claimed invention in not disclosing the steps of:

"providing a vapor deposition glass source"; "arranging the first substrate...be vapor coated"; and "vapor coating the first substrate side with a glass layer".

Camlibel discloses (Fig 5) encapsulating an analogous device (60) by e-beam deposition (col 4 ln 47), which inherently comprises providing a vapor deposition glass source, arranging the first substrate side in such a manner with respect to the vapor-deposition glass source that the first substrate side can be vapor coated, and vapor coating the first substrate side with a glass layer.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel by using e-beam deposition, as opposed to an adhesive; at least to prevent possible contamination from

the adhesive and further to eliminate an unnecessary layer which could interfere with light transmission and may not be as stable as the glass (Camlibel: col 1 ln 33-43).

Re claim 2, Wada discloses (Fig 9) the one or more regions are arranged on the first substrate side ([0084] ln 1-3).

Re claim 3, Wada discloses (Fig 9) providing the substrate with a passivation layer (26; [0136] ln 5) on a second side (A) that is on the opposite side from the first substrate side (B).

Re claim 4, Wada discloses the substrate comprises a wafer (5; [0083] ln 2), the process further comprising packaging components which still form part of the wafer ([00124] ln 1-5).

Re claim 5, Wada discloses coating a second substrate side with a protective film (26; [0136] ln 5).

Wada differs from the claimed invention in not disclosing vapor-coating a second substrate side with the glass layer.

Camlibel discloses (Fig 5) vapor coating (e-beam; col 4 ln 47) a second substrate side with the glass layer.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the process of Wada by using a glass layer, as taught by Camlibel, for the protective film (26); at least for the optical transmission properties (Camlibel: col 2 ln 48-50).

Re claim 6, Wada as modified above discloses the vapor-deposition glass source generates at least a binary glass system (borosilicate: Camlibel col 2 ln 55).

Re claim 7, Wada as modified above discloses the first substrate side is vapor-coated until the glass layer has a thickness in the range from 0.01 to 1000 μm (Camlibel col 7 ln 68; 3000 Angstroms = 0.3 μm).

Re claim 9, Wada as modified above discloses the glass layer has a thickness in the range between 0.1 and 50 μm (Camlibel col 7 ln 68).

Re claim 10, Wada as modified above differs from the claimed invention only in not expressly disclosing a glass layer thickness in the range between 50 and 200 μm.

Parameters such as film thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range between 50 and 200 μm; at least to optimize the glass layer's optical properties.

Re claim 11, Wada as modified above discloses generating a vapor from a glass target by means of an electron beam (inherent in e-beam; Camlibel col 4 ln 47).

Re claim 12, Wada as modified above does not limit the borosilicate glass to any particular type, therefore the combined disclosure encompasses all well-known borosilicate glass types, including those containing aluminum oxide and alkali metal oxide fractions.

Re claim 13, Wada as modified above discloses the glass layer has a coefficient of thermal expansion that is virtually equal to that of the substrate (Camlibel: col 2 ln 57-62; Fig 1, col 5 ln 7-18).

Re claim 14, Wada as modified above discloses the glass layer has a thickness sufficient to provide a hermetic seal (any thickness sufficient to encapsulate is regarded as being sufficient to provide a hermetic (air-tight) seal).

Re claim 16, Wada discloses (Fig 6F-6G) removing material from a second substrate side ([0091] ln 1-2), the second substrate side being on the opposite side from the first substrate side.

Re claim 17, Wada discloses (Fig 3) the substrate includes a wafer (5) having a plurality of the structures (3; [0083] ln 1-2) wherein the process further comprises dividing the wafer to form a plurality of electronic modules which each have first encapsulated sides ([0124] ln 1-5).

Re claim 38, Wada discloses (Fig 9) applying a ball grid array at the line contacts (24; col [0137] ln 2).

Re claim 18, Wada discloses (Fig 9) providing the underside with a plastic covering (26; [0135]) while leaving clear the ball grid array (24).

Re claim 39, Wada discloses (Figs 6) lithographing ([0085], [0089]) plastic layers (32, 42, 44) on the substrate to define the structure and removing the plastic layers from the underside (Fig 6F-6G: 44; [0091] ln 1-2).

Re claim 19, Wada as modified above discloses vapor coating the underside with the glass layer (Fig 11: 26) after the plastic layers (Fig 7F: 66) have been removed from the underside so that the plurality of electronic modules are encapsulated on both sides.

Re claim 40, Wada as modified above discloses (Fig 11A-11B) removing the plastic layers (26) from the underside comprises uncovering the line contacts (8,22) by local elimination of the glass layers (in going from Fig 11a to 11B).

Re claim 20, Wada as modified above differs from the claimed invention only in not expressly disclosing the glass layer on the underside has a thickness in the range from 1 to 50 μm.

Parameters such as film thickness in the art of semiconductor manufacturing are subject to routine experimentation and optimization.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range from 1 to 50; at least to optimize the glass layer's optical properties.

Re claim 21, Wada discloses (Fig 8A) filling in (interpreted as providing some amount of some filler) the etching pits with conductive material (8; [0098] ln 4-5).

Re claim 36, Wada discloses the etching pits are produced on the underside opposite the structure (Fig 8A: pits 4 are on underside A).

Re claim 37, Wada discloses the line contacts are produced on the underside opposite the structure (Fig 8A: contacts 8a are on underside A).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Camlibel as applied to claim 1 above, and further in view of Butt.

Re claim 8, Wada as modified above differs from the claimed invention only in not disclosing the step of "providing... formed on the first substrate side."

Butt discloses (Fig 1) electronic modules encapsulated with organic-reinforced glass (col 2 ln 67 – col 3 ln 6).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada as modified by Camlibel in view of Butt by providing a reservoir having organic constituents and converting the organic constituents into the vapor state through the application of a vacuum so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side; at least for reinforcing the glass (col 5 ln 11-15).

Claims 15, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Camlibel as applied to claim 1 above, and further in view of Xu.

Re claim 15, Wada as modified above differs from the claimed invention in not disclosing a plurality of glass layers.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 ln 51-53).

Xu discloses a dielectric stack of layers forming a partial mirror to reflect light (col 3 ln 35-44).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu by forming the glass layer from a plurality of glass layers; at least to reduce surface reflection.

Re claim 35, Wada as modified above discloses the plurality of glass layers have various glass compositions (Xu: col 3 ln 37-39).

Re claim 34, Wada as modified above differs from the claimed invention in not disclosing a layer of plastic above the glass layer.

Camlibel discloses using glass layers both as a dielectric mirror and to reduce reflection (col 3 ln 51-53).

Xu discloses a dielectric stack of layers forming a partial mirror to reflect light (col 3 ln 35-44).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada in view of Camlibel and Xu by forming a layer of plastic above the glass layer; at least to reduce surface reflection.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada in view of Camlibel as applied to claim 1 above, and further in view of Miles (US 2005/0244949).

Re claim 22, Wada as modified above differs from the claimed invention in not disclosing plasma ion assisted deposition.

Miles discloses ion assisted e-beam deposition controls stress ([0189] ln 11).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Wada as modified by Camlibel in view of Miles by using ion assisted e-beam deposition in place of conventional e-beam deposition; at least to control stress.

Response to Arguments

Applicant's arguments filed 08/24/2006 regarding claims 1-24, 26-32, and 34-40 have been fully considered but they are not persuasive.

Applicant's assertion that "Wada simply does not disclose or suggest thinning the wafer" is not persuasive. Applicant has presented neither evidence nor claim language to distinguish the invention as claimed from the reference as applied. Attorney arguments are not the kind of factual evidence that is required to rebut a *prima facie* case of obviousness. See MPEP § 2145(I). The term "thinning" must be given the broadest reasonable interpretation consistent with the specification. See MPEP § 904.01. The term "thinning" is not defined in applicant's specification (pg 8 ln 14-17).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "vapor coating...before the step of thinning") are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). See MPEP § 2145(VI).

Applicant's argument that "the cited art simply does not contain some suggestion or motivation to...prevent contamination" does not address the knowledge of persons of ordinary skill in the art. See MPEP § 2143.01(I). One skilled in the art would reasonably be expected to infer that, when using e-beam deposition, the adhesive layer is both unnecessary and a potential source of contamination. See MPEP § 2144.01.

Applicant's allegations of hindsight reasoning are not persuasive. Examiner's *prima facie* case of obviousness is based only knowledge within the level of ordinary skill in the art at the time the claimed invention was made. See MPEP § 2145(X)(B).

Examiner has considered the effect of applicant's claimed product-by-process limitations on the structure defined thereby. However, since the product in the product-by-process claim is the same as a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. See MPEP § 2113.

Applicant alludes to "distinctive structural features" that are not recited in the rejected claim. It is unclear that such features are in applicant's specification, however, limitations from the specification are not read into the claims. See MPEP § 2145(VI).

Applicant's arguments with respect to claim 25 have been considered but are moot in view of the new grounds of rejection.

Applicant's allegation that "the present application is in condition for allowance" is not persuasive. The ultimate determination of patentability is based on the entire record, by a preponderance of evidence. See MPEP § 2142(¶6). Rebuttal evidence is weighed against the evidence supporting the prima facie case. See MPEP § 716.01(d).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571- 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
13 November 2006

Sara Crane
Primary Examiner